Asst. Prof. ENGİN AFACAN

Personal Information

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Education Information

Doctorate, Bogazici University, Faculty Of Engineering, Department Of Electrıcal And Electronıcs Engıneerıng, Turkey 2009 - 2016
Postgraduate, Bogazici University, Instıtute Of Scıence, Elektrik-Elektronik Mühendisliği (Yl) (Tezli), Turkey 2008 - 2011

Foreign Languages

English, C2 Mastery

Dissertations

Doctorate, ANALOG CIRCUIT DESIGN AUTOMATION AGAINST PROCESSVARIATIONS AND AGING PHENOMENA, Boğaziçi Üniversitesi, Mühendislik Fakültesi, Elektrik-Elektronik Mühendisliği Bölümü, 2016

Research Areas

Engineering and Technology

Academic Titles / Tasks

Assistant Professor, Kocaeli University, Elektronik Ve Haberleşme Mühendisliği Bölümü, 2018 - 2021
Assistant Professor, Kocaeli University, Mühendislik Fakültesi, Elektronik Ve Haberleşme Mühendisliği Bölümü, 2017 - 2018
Research Assistant, Bogazici University, Faculty Of Engineering, Department Of Electrıcal And Electronıcs Engıneerıng, 2009 - 2015
Research Assistant, Bogazici University, Faculty Of Engineering, Department Of Electrıcal And Electronıcs Engıneerıng, 2009 - 2011

Articles Published in Journals That Entered SCI, SSCI and AHCI Indexes

I. **An efficient reliability simulation tool for lifetime-aware analog circuit synthesis**
Afacan E.
Turkish Journal Of Electrical Engineering And Computer Sciences, vol.1, no.1, pp.1-12, 2020 (Journal Indexed in SCI Expanded)
II. **On Chip Reconfigurable CMOS Analog Circuit Design and Automation Against Aging Phenomena: Sense and React**

AFACAN E., Dundar G., Baskaya F., Pusane A. E. , Yelten M. B.
ACM TRANSACTIONS ON DESIGN AUTOMATION OF ELECTRONIC SYSTEMS, vol.24, no.4, 2019 (Journal Indexed in SCI)

III. **A comprehensive analysis on differential cross-coupled CMOS LC oscillators via multi-objective optimization**
AFACAN E., Dundar G.
INTEGRATION-THE VLSI JOURNAL, vol.67, pp.162-169, 2019 (Journal Indexed in SCI)

IV. **Inversion coefficient optimization based Analog/RF circuit design automation**
AFACAN E.
MICROELECTRONICS JOURNAL, vol.83, pp.86-93, 2019 (Journal Indexed in SCI)

V. **A 10 GS/s time-interleaved ADC in 0.25 micrometer CMOS technology**
Aytar O., TANGEL A., AFACAN E.
JOURNAL OF ELECTRICAL ENGINEERING-ELEKTROTECHNICKY CASOPIS, vol.68, no.6, pp.415-424, 2017 (Journal Indexed in SCI)

VI. **Aging signature properties and an efficient signature determination tool for online monitoring**
Afacan E., Dundar G., Pusane A. E. , Yelten M. B. , Baskaya F.
INTEGRATION-THE VLSI JOURNAL, vol.58, pp.496-503, 2017 (Journal Indexed in SCI)

VII. **A lifetime-aware analog circuit sizing tool**
Afacan E., Berkol G., Dundar G., Pusane A. E. , Baskaya F.
Integration, vol.55, pp.349-356, 2016 (Journal Indexed in SCI)

VIII. **An analog circuit synthesis tool based on efficient and reliable yield estimation**
Afacan E., Berkol G., Dundar G., Pusane A. E. , Baskaya F.
Microelectronics Journal, vol.54, pp.14-22, 2016 (Journal Indexed in SCI)

IX. **Reliability assessment of CMOS differential cross-coupled LC oscillators and a novel on chip self-healing approach against aging phenomena**
Afacan E., Dundar G., Baskaya F.
Microelectronics Reliability, vol.54, no.2, pp.397-403, 2014 (Journal Indexed in SCI)

Articles Published in Other Journals

I. **Low Power-High Gain Bulk-Driven 3 Stages CMOS Miller OTA in 130nm technology**
AFACAN E.
Sakarya University Journal of Science, vol.24, no.5, pp.1113-1126, 2020 (Other Refereed National Journals)

Refereed Congress / Symposium Publications in Proceedings

I. **Improving POF Quality in Multi ObjectiveOptimization of Analog ICs via Deep Learning**
İslamoğlu G., Çakıcı O., AFACAN E., DÜNDAR G., Şeyda Nur G.
ECCTD2020, 7 - 10 September 2020

II. **Spiking Neuron Hardware-Level Fault Modeling**
Sarah E., Theofilos S., Pavlidis A., AFACAN E., Luis C., Baranco L., Haralampos S.
IOLTS2020, 13 - 15 July 2020

III. **Degradation Sensor Circuits for Indirect Measurements in Reconfigurable Analog Circuit Design**
AFACAN E., ateşavcı c.
ELECO2019, 28 - 30 November 2019

IV. **Artificial Neural Network Assisted Analog IC Sizing Tool**
AFACAN E., DÜNDAR G., İslamoğlu G., Çakıcı O.
SMACD2019, 15 - 18 July 2019

V. **Using Polynomial Regression and Artificial Neural Networks for Reusable Analog IC Sizing**

AFACAN E., DÜNDAR G.
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VI. **Post-silicon validation of yield-aware analog circuit synthesis**
AFACAN E., BERKOL G., DÜNDAR G.
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VII. **An Analog/RF Circuit Synthesis and Design Assistant Tool for Analog IP: DATA-IP**
AFACAN E., DÜNDAR G.
SMACD2018, 2 - 05 July 2018

VIII. **Variability Analysis Tool for CMOS Analog/RF Circuits: VariAnT**
AFACAN E.
SMACD2018, 2 - 05 July 2018

IX. **Design Space Exploration of CMOS Cross-Coupled LC Oscillators via RF Circuit Synthesis**
AFACAN E., DÜNDAR G.
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X. **A Rare Event Based Yield Estimation Methodology for Analog Circuits**
Odabaşı İ. Ç. , YELTEN M. B. , AFACAN E., BAŞKAYA İ. F. , PUSANE A. E. , DÜNDAR G.
2018 IEEE 21st International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS), Budapest, Hungary, 25 - 27 April 2018

XI. **Aging Aware Safe Operating Area Investigation of Switching Converter Output Stages Through 2D Plots**
AFACAN E., ozanoğlu k., toka m.
ICECS 2017, 4 - 08 December 2017

XII. **Inversion Coefficient Optimization Assisted AnalogCircuit Sizing Tool**
AFACAN E., DÜNDAR G.
SMACD 2017, 12 - 15 July 2017

XIII. **Review: Analog design methodologies for reliability in nanoscale CMOS circuits**
AFACAN E., YELTEN M. B. , DÜNDAR G.
2017 14th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Giardini Naxos, Italy, 12 - 15 June 2017

XIV. **ANALOG CIRCUIT DESIGN AUTOMATION AGAINST PROCESS VARIATIONS AND AGING PHENOMENA**
AFACAN E.
DATE 2017, 27 - 31 March 2017

XV. **A Hierarchical Design Automation Concept for Analog Circuits**
BERKOL G., AFACAN E., Fernandez F., DÜNDAR G.
IEEE International Conference on Electronics, Circuits and Systems, At Monte Carlo, 12 - 14 December 2016

XVI. **Efficient signature selection tool for sense react systems**
AFACAN E., DÜNDAR G., PUSANE A. E. , BAŞKAYA İ. F. , YELTEN M. B.
Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2016 13th International Conference on, 27 - 30 June 2016

XVII. **Semi empirical aging model development via accelerated aging test**
AFACAN E., DÜNDAR G., PUSANE A. E. , BAŞKAYA İ. F.
Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2016 13th International Conference on, 27 - 30 June 2016

XVIII. **A Mixed Domain Sizing Approach for RF Circuit Synthesis**
AFACAN E., DÜNDAR G.
The IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems, 20 - 22 April 2016

XIX. **A deterministic aging simulator and an analog circuit sizing tool robust to aging phenomena**
AFACAN E., BERKOL G., DÜNDAR G., BAŞKAYA İ. F. , PUSANE A. E.
SMACD 2015, 7 - 09 September 2015

XX. **A two step layout in the loop design automation tool**

BERKOL G., Unutulmaz A., AFACAN E., DÜNDAR G., V Fernandez F., PUSANE A. E. , BAŞKAYA İ. F.
NEWCAS 2015, 7 - 10 June 2015

XXI. **A novel yield aware multi objective analog circuit optimization tool**
BERKOL G., AFACAN E., DÜNDAR G., PUSANE A. E. , BAŞKAYA İ. F.
ISCAS 2015, 24 - 27 May 2015

XXII. **A hybrid Quasi Monte Carlo method for yield aware analog circuit sizing tool**
AFACAN E., BERKOL G., DÜNDAR G., PUSANE A. E. , BAŞKAYA İ. F.
DATE 2015, 9 - 13 March 2015

XXIII. **Sensitivity based methodologies for process variation aware analog ic optimization**
AFACAN E., BERKOL G., BAŞKAYA İ. F. , DÜNDAR G.
PRIME 2014, 30 June - 02 July 2014

XXIV. **Model based hierarchical optimization strategies for analog design automation**
AFACAN E., Ay S., V Fernandez F., DÜNDAR G., BAŞKAYA İ. F.
DATE, 24 - 28 March 2014

XXV. **A High Speed Low Power CMOS Current Comparator**
AFACAN E., TANGEL A., AYTAR O.
IEEJ, 17 July 2008 - 21 March 2014

XXVI. **Reliability enhancement using in field monitoring and recovery for RF circuits**
Özev S., Chang D., Bakkaloğlu B., Kiaei S., AFACAN E., DÜNDAR G.
VTS 2014, 13 - 17 April 2014

XXVII. **Adaptive sized quasi monte carlo based yield aware analog circuit optimization tool**
AFACAN E., BERKOL G., DÜNDAR G., PUSANE A. E. , BAŞKAYA İ. F.
VARI, 29 September 2014 - 01 October 2013

XXVIII. **An FPGA based multiple output PWM pulse generator for ultrasonic cleaning machines**
Tangel A., Yakut M., Afacan E., Güvenç U.
Applied Electronics, Plzen, Czech Republic, 8 - 09 September 2010

XXIX. **YÜKSEK HIZLI CMOS AKIM KARŞILAŞTIRICI**
AFACAN E., AYTAR O., TANGEL A.
12.EEBB, Turkey, 13 - 17 November 2007

Supported Projects

AFACAN E., Project Supported by Higher Education Institutions, ANALOG CMOS TÜMDEVRELER İÇİN ALGILA VE UYARLA SİSTEMİ TASARIM OTOMASYONU, 2018 - 2020
TUBITAK Project, Yaşlanma ve ğarametre saçılımna karşı gürbüz analog devre tasarım otomasyonu, 2013 - 2017

Citations

Total Citations (WOS):34
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